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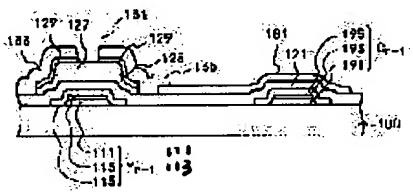
(54) SEMICONDUCTOR DEVICE AND ITS PRODUCTION

(57)Abstract:
PURPOSE: To obtain a semiconductor device which is sufficiently lowered in the wiring resistance of main scanning line and is not degraded in production yield even under severe production conditions by providing the scanning lines with first metallic layers consisting essentially of aluminum, alloy layers and second metallic layers.
CONSTITUTION: An array substrate for an active matrix type display device has signal lines and the scanning lines Yn-1 intersecting orthogonally with the signal lines on a transparent glass substrate 100. The scanning lines Yn-1 includes the first metallic layers 111 consisting of the pure aluminum(Al), the second metallic layers 113 consisting of molybdenum(Mo) arranged on the upper layers of the metallic layers 111 and the alloy layers 115 consisting of Mo- tungsten (W) alloy covering the metallic layers 111, 113. As a result, the wiring resistance of the scanning lines Yn-1 themselves is sufficiently lowered and the hillocks and round bulging of the scanning lines themselves or the degradation in the production yield by insulation defects, etc., are lessened.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor device which a non-single-crystal-silicon thin film is arranged, and changes on an insulating substrate, and its manufacture technique.
[0002]
[Description of the Prior Art] Conventionally, since the semiconductor device with which non-single-crystal-silicon thin films, such as amorphous silicon (it is hereafter called a-Si:H for short.) and polycrystal silicon (it is hereafter called p-Si for short.), were used as a semiconductor thin film can be comparatively formed over a large area on an insulating substrate at homogeneity, it is used for a pixel switch or a drive circuit of active matrix type display etc.
[0003] If it is in such a semiconductor device, using low resistance metals, such as aluminum (aluminum), for the scanning line, for example is known from the need that the scanning line is fully low resistance.
[0004] However, if aluminum (aluminum) is used as scanning line, a hillock etc. will occur in a wiring, the problem referred to as a poor insulation arising in the gate insulator layer of a semiconductor device and the insulator layer for an intersection of the scanning line and a signal line, or causing the poor element of a semiconductor device will arise, and the manufacture yield will fall sharply.
[0005] Then, by covering an aluminum (aluminum) wiring with a metal or aluminium alloys, such as chromium (Cr) which has a high-melting point from aluminum (aluminum), a tungsten (W), titanium (Ti), or a tantalum (Ta), etc., the hillock of an aluminum (aluminum) wiring is prevented to JP,4-353830,A, JP,5-152572,A, or JP,6-120503,A, and the semiconductor device which solves the above-mentioned trouble is indicated.
[0006]
[Problem(s) to be Solved by the Invention] By the way, non-single-crystal-silicon thin films, such as a-Si:H and p-Si, activate reactant gas by energy, such as heat, light, or a plasma, and are formed by the CVD system.
[0007] In recent years, in order to improve a productivity, especially membrane formation conditions, such as temperature, are a severe condition much more for the scanning line which made aluminum (aluminum) the subject. Such inside, if it is in the above-mentioned structure, the hillock still generated in an aluminum (aluminum) wiring is fully unmitigable, for this reason, a big constraint will be received in a manufacture process, and the manufacture yield will be reduced.
[0008] This invention copes with the above-mentioned technical technical probrem, and is accomplished, wiring resistance of the scanning line is fully reduced, and moreover, even if it is severe manufacture conditions, it aims at offering the semiconductor device with which the manufacture yield does not fall, and its manufacture technique.
[0009]
[Means for Solving the Problem] In the semiconductor device equipped with the source electrode and drain electrode which are electrically connected to the insulator layer with which invention indicated by the claim 1 covers the scanning line and the aforementioned scanning line on an insulating substrate, the non-single-crystal-silicon thin film arranged through the aforementioned insulator layer on the aforementioned scanning line, and the aforementioned non-single-crystal-silicon thin film The aforementioned scanning line is characterized by having the 2nd metal layer which made the principal component one element which constitutes the aforementioned alloy layer arranged between the 1st metal layer which makes aluminum (aluminum) a principal component, the alloy layer which covers the aforementioned 1st metal layer, and the aforementioned 1st metal layer and the aforementioned alloy layer.
[0010] Invention indicated by the claim 2 is characterized by the aforementioned alloy layer being a molybdenum (Mo)-tungsten (W) alloy or a molybdenum (Mo)-tantalum (Ta) alloy in the semiconductor device according to claim 1.
[0011] Invention indicated by the claim 3 is characterized by the aforementioned 2nd metal layer making molybdenum (Mo) a principal component in the semiconductor device according to claim 2. Moreover, the 1st metal layer to which invention indicated by the claim 4 makes aluminum (aluminum) a principal component on an insulating substrate, The scanning line containing the 2nd metal layer which made the principal component one element which constitutes the aforementioned alloy layer arranged between the alloy layer which covers the aforementioned 1st metal layer, and the aforementioned 1st metal layer and the aforementioned alloy layer, It is the manufacture technique of the semiconductor device equipped with the source electrode and drain electrode which are electrically connected to the insulator layer which covers the aforementioned scanning line, and the non-single-crystal-silicon thin film and the aforementioned non-single-crystal-silicon thin film which are arranged through the aforementioned insulator layer on the aforementioned scanning line. The process which deposits the 2nd metal

membrane which made the principal component the one aforementioned element which constitutes the 1st metal membrane and the aforementioned alloy layer which make aluminum (aluminum) a principal component on the aforementioned insulating substrate, the 1st aforementioned metal membrane and the 2nd aforementioned metal membrane -- patterning -- carrying out -- the [the 1st metal layer and] -- it is characterized by constituting the aforementioned scanning line according to the process which forms 2 metal layer, the process which deposits the alloy layer which covers the aforementioned 1st metal layer and the aforementioned 2nd metal layer, and the process which carries out patterning of the aforementioned alloy layer

[0012]

[Function] In the semiconductor device and its manufacture technique of this invention, a characteristic thing has the scanning line in having the 2nd metal layer which made the principal component one element which constitutes the alloy layer arranged between the 1st metal layer which makes aluminum (aluminum) a principal component, the alloy layer which covers the 1st metal layer, and the 1st metal layer and an alloy layer, as mentioned above.

[0013] since the 1st metal layer which constitutes the scanning line makes aluminum (aluminum) the principal component, wiring resistance of the scanning line [itself] can fully be reduced, and it cuts that this makes a waveform distortion to be generated to a scanning pulse Therefore, the write-in time of the video signal to a pixel electrode does not differ greatly by the side far from an electric supply [of a scanning pulse], and electric supply side, and a good display image can be realized.

[0014] By the way, aluminum (aluminum) is an activity metal and the 1st metal layer which makes this aluminum (aluminum) a principal component is easy to be corroded to the chemical used at a back process. According to this invention with a deer deer, since the 1st metal layer is fully covered with the alloy layer, it does not cause the cauterization of the 1st metal layer.

[0015] By the way, as an alloy layer, if the resistance and chemical resistance are taken into consideration, a molybdenum (Mo)-tungsten (W) alloy or a molybdenum (Mo)-tantalum (Ta) alloy is used suitably, and the molybdenum (Mo)-tungsten (W) alloy is especially suitable especially. Moreover, this alloy layer not only protects the 1st metal layer from a chemical etc., but acts so that round-head bulging by the hillock of the 1st metal layer or the influence of asymmetry may be prevented.

[0016] However, if it is fully going to prevent the hillock and round-head bulging of the 1st metal layer only in this alloy layer, you have to set the thickness of an alloy layer as the thick film of 10 times or more of the thickness of the 1st metal layer. However, in order for membrane formation to take a long time to such an alloy layer of a thick film, to increase the thickness of the scanning line it not only to to spoil a productivity, but and to produce a card row piece, a poor insulation, etc. of a wiring by this level difference, a creation of the semiconductor device which used the scanning line itself as the gate electrode becomes completely difficult.

[0017] Since it is such, in this invention, it is characterized by having the 2nd metal layer which made the principal component one element which constitutes an alloy layer between the 1st metal layer and an alloy layer further. By arranging the 2nd metal layer, it is effectively prevented by the grade which makes stress concentration ease that a hillock produces an alloy layer in the 1st metal layer also as a thin film. The effect was checked, even if this 2nd metal layer covered the 1st metal layer completely and it had been again arranged only on the main front face of the 1st metal layer.

[0018] As the 2nd metal layer arranged on the 1st metal layer In order to prevent the hillock and round-head bulging of the 1st metal layer which make aluminum (aluminum) a principal component and to secure an alloy layer and sufficient adhesion moreover, If an alloy layer is a molybdenum (Mo)-tungsten (W) alloy or a molybdenum (Mo)-tantalum (Ta) alloy as it is necessary to make into a principal component one element which constitutes an alloy layer and it was described above The metal layer which makes molybdenum (Mo) a principal component is suitably used for the 2nd metal layer.

[0019] If molybdenum (Mo) is especially constituted for the 2nd metal layer as a principal component, patterning of the 1st metal layer can be carried out to a taper configuration by setting up the etching rate of the 2nd metal layer highly, and etching in case of patterning of the 1st metal layer, compared with the etching rate of the 1st metal layer. This does so the effect that dielectric breakdown in the level difference fraction of the scanning line and occurrence of card row piece ****** of a wiring are fully mitigable.

[0020] Furthermore, if a molybdenum (Mo)-tungsten (W) alloy or a molybdenum (Mo)-tantalum (Ta) alloy is constituted for an alloy layer and molybdenum (Mo) is constituted for the 2nd metal layer as a subject, the adhesion of the 2nd metal layer and an alloy layer can be raised, and contact resistance can also be reduced. Moreover, if constituted like the above, the scanning line containing three layers can consist of two patterning.

[0021]

[Example] The array substrate for active matrix type display for which the semiconductor device of one example of this invention was used is hereafter taken for an example, and it explains with reference to a drawing. drawing 1 -- array substrate (1) for active matrix type display of this example it is outline front view a part and drawing 2 was cut along with the A-A' line in drawing 1 -- it is an outline cross section in part

[0022] This array substrate for active matrix type display (1) Transparent glass substrate (100) It has upwards 640x3 signal lines Xi (i= 1, 2, --, m and --, 1920) and the 480 scanning lines Yj (j= 1, 2, --, n and --, 480) which intersect perpendicularly with this signal line Xi. And transparent pixel electrode which consists of I.T.O. (Indium Tin Oxide) in the field surrounded by each signal line Xi and the scanning line Yj (181) It is arranged and constituted.

[0023] TFT of the reverse stagger structure which used the scanning-line Yj itself as the gate electrode at a part for the intersection of each signal line Xi and each scanning line Yj (131) It is arranged. This TFT (131) As shown in drawing 2 , on the scanning line Yj The insulator layer of the laminated structure of a silicon-oxide (SiO2) layer and a silicon-nitride (SiNx) layer (121), Insulator layer (121) The semiconductor thin film (125) which consists of the a-Si:H thin film arranged upwards, Semiconductor thin film (125) The channel protective coat by which has been arranged upwards and self-matching was carried

out at the scanning line Yj (127), Semiconductor thin film (125) Low resistance semiconductor layer (129) Source electrode which minds and is connected electrically (135) And a signal line Xi and the drain electrode of one (133) It is arranged and changes.
[0024] Moreover, 480 supplementary capacity lines Cj are allotted to the scanning line Yj and abbreviation parallel, and it is an insulator layer (121). Pixel electrode allotted by minding (181) Supplementary capacity (Cs) is formed by the supplementary capacity line Cj.
[0025] by the way, the 1st metal layer (111) with a wiring width of face [to which the scanning line Yj of this example changes from pure aluminum (aluminum)] of 8 microns this 1st metal layer (111) The 2nd metal layer (113) which consists of the molybdenum (Mo) arranged at the upper layer the [the 1st and] -- 2 metal layer (111) (113) Alloy layer (115) with a wiring width of face [which consists of the molybdenum (Mo)-tungsten (W) alloy to cover] of 14 microns It contains. It is an alloy layer (115) here. It is the 1st metal layer (111) about wiring width of face. Compared with wiring width of face, set up greatly. the [namely,] -- 1 metal layer (111) A wiring edge to alloy layer (115) having made 3 microns extend at a time -- alloy layer (115) even if a gap etc. arises in patterning -- the 1st metal layer (111) It is for giving additional coverage to position doubling so that it may be covered completely. In addition, since the supplementary capacity line Cj is also the same structure, an explanation is omitted.
[0026] The 1st metal layer of the scanning line Yj (111) And the 1st metal layer of the supplementary capacity line Cj (191) It has a 2000A thickness, respectively, and is the 2nd metal layer (113) of the scanning line Yj. And the 2nd metal layer of the supplementary capacity line Cj (193) 500A and alloy layer of the scanning line Yj (115) And alloy layer of the supplementary capacity line Cj (195) It has the 3000A thickness, respectively.
[0027] The 1st metal layer of the scanning line Yj (111) It is the main wiring which constitutes the scanning line Yj, and even if it is ********, in order to attain sufficient low resistance-ization, it is desirable to consider as a 1000-3000A thickness. If a thickness is thinner than 1000A, sufficient low resistance-ization will not be attained, and if 3000A is exceeded, the level difference of the scanning line Yj will become large, and there is a possibility of causing a poor insulation near the level difference section.
[0028] The 2nd metal layer of the scanning line Yj (113) The 1st metal layer (111) Alloy layer (115) It functions as raising the adhesion of a between and easing stress, and sufficient effect will be acquired if it is 300A or more according to this invention person's etc. experiment.
[0029] Moreover, alloy layer of the scanning line Yj (115) The 1st metal layer (111) It reaches, the 2nd metal layer (113) is covered completely, and, moreover, it is the 1st metal layer (111). It is desirable to set it as a 2000-4000A thickness so that occurrence of a hillock or round-head bulging may be prevented.
[0030] Moreover, since the supplementary capacity line Cj is the same as that of the scanning line Yj, an explanation is omitted. Array substrate for active matrix type display constituted as mentioned above (1) When depending, wiring resistance of the scanning-line Yj [itself] was fully able to be reduced with 7kohm by 21cm.
[0031] Moreover, array substrate for active matrix type display of this example (1) When depending, the fall of the manufacture yield was mitigated by the hillock of the scanning line [itself], round-head bulging or a poor insulation, etc.
[0032] And according to such a configuration, the durability test of 50 degrees C, for example, temperature, and ** which does not have a picture image degradation in RH environment 80% of humidity were checked as a LCD. Furthermore, according to this invention, it is each TFT (131). It was also checked that mobility can improve. Below, it explains with reference to drawing 3.
[0033] TFT of this example (131) Channel protective coat (127) Self-matching is carried out to the scanning line Yj, and since it is constituted, it has the channel length (LC) of 12 microns of every 1 micron parvus from the scanning line Yj to the scanning-line width of face (LG) of the scanning line Yj. Moreover, the scanning line Yj is the three-tiered structure which was mentioned above, and the level difference sections A and B are formed in channel length (LC), respectively.
[0034] And in this example, the distance (delta 1) of the level difference sections A and B and a channel-length (LC) edge and (delta 2) especially approach 2 microns and a channel-length (LC) edge, respectively, and it is arranged.
[0035] Therefore, these level difference sections A and B are insulator layers (123). Although it is not so steep as a poor insulation is caused, it is a semiconductor thin film (125) near the channel-length (LC) edge. It receives, and in order to function as fully centralizing the electric field, mobility fully improves, without causing increase of a leakage current.
[0036] According to this invention person's etc. experiment, that especially the thing set to or less channel-length (LC) *1/4, respectively is desirable made clear the distance (delta 1) of the level difference sections A and B and a channel-length (LC) edge, and (delta 2) to channel length (LC).
[0037] Next, array substrate for active matrix type display of this example (1) A manufacture process is explained briefly. First, as shown in drawing 4 (a), it is a glass substrate (100). On 1 principal plane, an aluminum (aluminum) layer and a molybdenum (Mo) layer are deposited by the spatter so that it may become a thickness (2000A and 500A) one by one. After allotting and developing [expose and] a photoresist, then, by etching using the mixed acid of a phosphoric acid, an acetic acid, and a nitric acid A side etch goes into a molybdenum (Mo) layer from the difference of the etching rate of an aluminum (aluminum) layer and a molybdenum (Mo) layer. The taper-like 1st metal layer (191) (193) (111) (191), It reaches and is the 1st metal layer (111). The 2nd metal layer arranged only on the top (113), It obtains. In addition, although not illustrated, the 1st-mask alignment mark which consists of an aluminum (aluminum) layer and a molybdenum (Mo) layer simultaneously is formed.
[0038] the [then,] -- 1 metal layer (111) (191) the [a side attachment wall and] -- 2 metal layer (113) -- (193) A molybdenum (Mo)-tungsten (W) alloy layer is deposited by the spatter so that it may cover. As allot a photoresist, it carries out position

doubling to the above-mentioned mask position doubling mark, is exposed and developed, par ******** of the molybdenum (Mo)-tungsten (W) alloy layer is carried out and it is shown in drawing 4 (b) The 1st metal layer (193) (195) (111) (191), It reaches and is the 2nd metal layer (113). Alloy layer (115), Scanning-line Yn-1 of a three-tiered structure It obtains. In addition, simultaneously with the above-mentioned process, it is scanning-line Yn-1. Supplementary capacity line Cn-1 of the same three-tiered structure It obtains. Moreover, although not illustrated, the 2nd-mask alignment mark is formed simultaneously with patterning of a molybdenum (Mo)-tungsten (W) layer, and subsequent exposure is performed based on the 2nd-mask alignment mark.

[0039] Thus, the scanning line n-1 formed And supplementary capacity line Cn-1 A silicon-oxide (SiO2) layer is deposited upwards. Moreover, although not illustrated, it is a substrate (100) in the reactor of a CVD system. It arranges and is a reactor (113) as reactant gas about the silane (SiH4) of the flow rate of 200sccms, the ammonia (NH3) of the flow rate of 1000sccm, and the nitrogen (N2) of the flow rate of 7000sccm. While introducing inside, the inside of a reactor is maintained to 1Torr, and glass-substrate temperature is further raised to 330 degrees C. And the high-frequency voltage of 1300W is supplied, plasma excitation of a silane (SiH4) and the ammonia (NH3) is carried out by this, and a silicon nitride (SiNx) is made to deposit by the 500A thickness. Thus, insulator layer of the laminated structure of the silicon-oxide (SiO2) layer and silicon nitride (SiNx) which are shown in drawing 4 (c) (121) Scanning line n-1 And supplementary capacity line Cn-1 It deposits upwards.

[0040] then, the inside of the same reactor -- reactant gas -- the silane (SiH4) of the flow rate of 400sccms, and the hydrogen (H2) of the flow rate of 1400sccm -- gas -- switching -- the inside of a reactor -- introducing -- further -- the RF power of 150W -- supplying -- insulator layer (121) a top -- a-Si:H thin film (123) It is made to deposit by the 500A thickness. In addition, even if it faces deposition of an a-Si:H thin film (123), the inside of a reactor is maintained to 1Torr.

[0041] While it is introduced into the silane (SiH4) of the flow rate of 200sccms, and the ammonia (NH3) of the flow rate of 1000sccm as reactant gas and the nitrogen (N2) of the flow rate of 7000sccms is introduced in a reactor as carrier gas, the high-frequency voltage of 1300W is supplied and a silicon nitride (SiNx) is made to deposit by the 3000A thickness again. In addition, even if it faces deposition of a silicon nitride (SiNx), the inside of a reactor is maintained to same 1Torr.

[0042] Then, substrate (100) It takes out out of a reactor, a photoresist is applied on a silicon nitride (SiNx), and it is a glass substrate (100). At irradiating rear-face light, it is scanning-line Yn-1. Channel protective coat which the exposure by which self-matching was carried out accomplishes, develops and carries out patterning, and is shown in drawing 4 (c) (127) It obtains.

[0043] Next, a-Si:H thin film (123) Patterning is carried out to the shape of an island, and it is a semiconductor thin film (125). It carries out. And as shown in drawing 4 (d), it arranges in a CVD system, and patterning of the n+a-Si:H thin film is deposited and carried out, and it is an island-like n+a-Si:H thin film (128). It carries out, and further, membranes are formed, patterning of the I.T.O. layer is carried out, and it is a pixel electrode (181). It forms.

[0044] Furthermore, as patterning of the aluminum is put and carried out and it is shown in drawing 2 , they are a source electrode (135), a drain electrode (133), and a source electrode (135). The low resistance semiconductor layer (129) arranged between semiconductor thin films (125), and drain electrode (133) Semiconductor thin film (125) Low resistance semiconductor layer arranged in between (129) It obtains.

[0045] According to the manufacture technique mentioned above, the effect that the scanning line Yj of a three-tiered structure can be well formed in the shape of a taper by two patterning is done so. Moreover, each class which constitutes the scanning line Yj is deposited, respectively, and may carry out patterning individually. However, since it is necessary to take the doubling precision of each class into consideration by such manufacture technique, as wiring resistance to the wiring width of face of the scanning line Yj, the above-mentioned manufacture technique is advantageous. Moreover, according to the above-mentioned manufacture technique, since the level difference section of the scanning line Yj approaches a channel-length (Lc) edge and can arrange, compared with carrying out patterning of each class which constitutes the scanning line Yj individually, respectively, high mobility is securable.

[0046] Although the above-mentioned example explained for the example the case where a-Si:H was used as a semiconductor thin film, it cannot be overemphasized that you may be p-Si and may be microcrystal silicon etc.

[0047]

[Effect of the Invention] According to the semiconductor device and its manufacture technique of this invention, wiring resistance of the scanning line is fully reduced, and moreover, the productivity which was therefore excellent can be secured, without the manufacture yield falling, even if it is severe manufacture conditions. Moreover, according to the manufacture technique of this invention, the semiconductor device with which the wiring resistance of the scanning line without a fall of the manufacture yield was fully reduced is obtained with the few number of patterning.

[Translation done.]